ABSTRACT OF THE DISCLOSURE

Clock circuitry supplies synchronized clock waves to loads on plural integrated circuit chips. The clock circuitry couples the synchronized clock waves to regions of the chips. There is a first clock wave route in a first direction from a first chip to a second chip and a second clock wave route in a second direction from the second chip to the first chip. The routes have substantially the same geometry and are in close proximity to each other so they have substantially the same effects on clock waves propagating therein in opposite directions. A phase detector and lowpass filter on the first chip responds to (1) a clock wave source and (2) a clock wave derived on a chip other than the first chip, to supply, via a common mode line, a control for voltage controlled delays of the chips other than the third chip.